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EXAMINER
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ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	**Application No.** 09/881,254	**Applicant(s)** HSHIEH ET AL.	
	Examiner Johannes P Mondt	**Art Unit** 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/28/03 has been entered.

Response to Amendment

Amendment B as proposed and filed 04/10/03 has been entered as Paper No. 10 in view of above mentioned Request for Continued Examination. Comments on Remarks by Applicant are included below in "Response to Arguments".

Response to Arguments

2. Applicant's arguments filed 04/10/03 have been fully considered but they are not persuasive. A uniform concentration profile as taught by Vinson is one example of a symmetric profile. Vinson thus teaches his profile for retaining electrical symmetry (cf. col. 6, lines 28-32), while this profile satisfies the claim language. The substantially amended claim language as introduced in said Amendment B distinguishes the claimed invention over Mogi et al and Vinson; however, the application of ion implantation of the body region in a trench-gated MOSFET as taught by Darwish (6,569,738 B2) for the specific purpose of inter alia increased breakdown voltage (cf. abstract) combines well

with the teaching by Vinson, as the body region's dopant concentration profile as given by Figure 8A is substantially symmetric and relatively flat in the middle, while it is understood in the art that any electrical asymmetry necessarily tends to decrease breakdown voltage. Furthermore, by increasing the overall level of dopant concentration Darwish accomplishes a reduction in any *relative* asymmetry. In this regard the profile by Darwish does not distinguish over that in Figures 7 or 11 of the disclosure, although other figures in said disclosure such as Figures 8 and 9 show a substantially peaked central region of the p-body dopant concentration profile, distinguished from Darwish. Applicant is encouraged to explore patentability on this distinction.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1 – 4, 6 – 8, 10 – 16 and 26*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al (4,250,519) in view of Vinson (4,116,720) and Darwish (6,569,738 B2).

With regard to claims 1 – 3: With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:

a drain region 24 (cf. column 3, lines 3-5) of first conductivity type (n type);

a body region 26 of second conductivity type (p type) provided over said drain region, said drain region and said body region forming a first junction;

a source region 27 (cf. column 3, lines 13-14) of first conductivity type provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region 27, through said body region 26 and into said drain region 24 (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising an insulating layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a conductive region 32 (cf. column 3, line 20) within said trench adjacent said insulating layer, and in which gate region gate metal, particularly aluminum metal (cf. column 3, line 21) is allowed to be adjacent said conductive region (the additional limitation as defined by *claim 3* is thus anticipated by Mogi et al).

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3) (the additional limitation as defined by *claim 2* is thus anticipated by Mogi et al).

Mogi et al do not necessarily teach the further limitation defined ad (b) in claim 1 of Applicants. *However,* in a patent on a vertical MOSFET with groove

alias trench (cf. title and abstract) and *for the specific purpose of retaining electrical symmetry (cf. column 6, line 32)*, Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer without additional doping with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32).

Although neither Mogi et al nor Vinson necessarily teach a non-uniform doping profile in the body region, *Darwish teaches* that inter alia for increased breakdown voltage the body region 34 (cf. column 4, lines 20-30) in a trench-gated MOSFET should be additionally p-doped; the general characteristics of a flat and symmetric profile are retained in a central portion of the p-body region (cf. Figure 8A and column 4, lines 63-65), but the concentration is higher through said additional doping, and thus, inherently, given any density fluctuation the relative deviation from electrical symmetry is lower than without said additional doping step because of the increased screening.

Motivation to include the teaching by Vinson is the benefit of higher breakdown voltage flowing from electrical symmetry, while the additional teaching by Darwish substantially retains said symmetry while diminishing the effects of asymmetry further by increasing the level of doping in the central

portion of the body region. *Combination* of the teachings by Vinson and Darwish with Mogi et al is straightforward because Mogi et al already use ion implantation for creating the source and drain regions. *Success* in implementing the combination can therefore be reasonably expected.

With regard to claim 4: body region 26 in Mogi et al is a lightly P-doped semiconductor (epitaxial) layer (cf. column 3, lines 5-6), any doped semiconductor region has dopants, while each dopant is a generation-recombination center. Thus the further limitation of claim 4 does not distinguish from the prior art as taught by Mogi et al.

With regard to claim 6: source, drain, and body regions as taught by Mogi et al are doped silicon regions (cf. column 2, line 61 – 63, column 3, lines 13 – 14 and 24). Therefore, the further limitation as defined by claim 6 does not distinguish over the prior art as taught by Mogi et al.

With regard to claim 7: said conductive region 32 as taught by Mogi et al can be made of polysilicon (cf. column 3, lines 20-23). Therefore, the further limitation as defined by claim 7 does not distinguish over the prior art as taught by Mogi et al.

With regard to claim 8: said insulating layer 29 as taught by Mogi et al is a silicon dioxide layer (cf. column 3, lines 22-23). Therefore, the further limitation as defined by claim 8 does not distinguish over the prior art as taught by Mogi et al.

With regard to claim 10: the examiner takes official notice that in general, a gate insulator layer of silicon dioxide formed using CVD or PVD has many dangling bonds within the film. These become interface states or fixed charges within the insulating layer. Applicants' further limitation as defined by claim 10 is therefore a result of standard fabrication procedures of said insulating layer and does not distinguish over the prior art.

With regard to claim 11: said source and drain regions as taught by Mogi et al, as well as by Vinson, as well as by Darwish are heavily doped regions with peak net doping concentrations greater than a peak net doping concentration of the body region (region 26 is lightly p-doped, regions 24 and 27 heavily n-doped in Mogi et al; source and drain regions 22 and 25 are heavily n-doped and body region 21 is lightly p-doped in Vinson; for Darwish see Figure 8A).

With regard to claim 12: said first conductivity type taught by Mogi et al is n type and said second conductivity type as taught by Mogi et al is p type, as detailed above in the discussion of claim 1. Therefore, the further limitation as defined by claim 12 does not distinguish over the prior art as taught by Mogi et al.

With regard to claim 13: Mogi et al teach that said source and drain regions 27 and 24 comprise the same dopant, namely phosphorus (cf. col. 3, lines 40-45).

With regard to claim 14: With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:

a silicon drain region 24 (column 3, lines 13-14) of N-type conductivity;

a silicon body region 26 of P-type conductivity (cf. column 3, lines 5-6) provided over said drain region, said drain region and said body region forming a first junction;

a silicon source region 27 (cf. column 3, lines 3-4) of N-type conductivity provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region, through said body region and into said drain region (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising a silicon dioxide layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a doped polycrystalline silicon region 32 (cf. column 3, line 20) within said trench adjacent said silicon dioxide layer,

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3). In the invention taught by Mogi et al the source and drain region have peak doping densities high (cf. column 3, lines 13-14) compared with the doping density of the (epitaxial) body region 26 (cf. column 3, line 46) and comprise the same doping material, namely phosphorus (cf. col. 3, lines 40-45).

Mogi et al do not necessarily teach the further limitation defined by (d).

However, for the specific purpose of retaining electrical symmetry (cf. column 6, line 32), Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer (cf. column 3, lines 5-6 and line 24) and with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32).

Although neither Mogi et al nor Vinson necessarily teach a non-uniform doping profile in the body region, *Darwish teaches* that inter alia for increased breakdown voltage the body region 34 (cf. column 4, lines 20-30) in a trench-gated MOSFET should be additionally p-doped; the general characteristics of a flat and symmetric profile are retained in a central portion of the p-body region (cf. Figure 8A and column 4, lines 63-65), but the concentration is higher through said additional doping, and thus, inherently, given any density fluctuation the

relative deviation from electrical symmetry is lower than without said additional doping step because of the increased screening.

Motivation to include the teaching by Vinson is the benefit of higher breakdown voltage flowing from electrical symmetry, while the additional teaching by Darwish substantially retains said symmetry while diminishing the effects of asymmetry further by increasing the level of doping in the central portion of the body region. *Combination* of the teachings by Vinson and Darwish with Mogi et al is straightforward because Mogi et al already use ion implantation for creating the source and drain regions. *Success* in implementing the combination can therefore be reasonably expected.

With regard to claims 15-16: Mogi et al use phosphorus as n-type doping material for both source 27 and drain 24 (cf. column 3, lines 40-45 and lines 57-60) (claim 16). Although Mogi et al do not necessarily teach arsenic for both source and drain (only for source 27; cf. col. 3, lines 57-60), the examiner takes official notice that arsenic is desired for steeper profiles because of its low diffusion speed (higher mass number) while steeper profiles diminish the spatial range on the border between source/drain and body region where small fluctuations have a relatively large effect on the electric field because of reduced screening. For these reasons it would have been obvious to include arsenic as dopant for both source and drain (claim 15), as taught by Darwish (cf. column 4, lines 51-65).

With regard to claim 26: Mogi et al do teach the trench MOSFET transistor device to comprise a plurality of source regions shorted to one another, specifically the source regions 23 contacting the respective bottom portions of the trenches of trench MOS transistor devices 38 and 39.

3. ***Claim 5** is rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al, Vinson and Darwish as applied to claim 4 above, and further in view of Seki (5,025,293).

As detailed above, claim 4, on which claim 5 depends, is unpatentable over Mogi et al in view of Vinson and Darwish, none of whom, however, necessarily teach the further limitation as defined by claim 5. *However, the use of gold, or as a non-exclusive alternative platinum*, as a dopant in semiconductor material as a material to provide generation-recombination centers *for the purpose of shortening charge carrier lifetime and thereby reducing turn-off time* has long been known in the art of semiconductor device technology, as witnessed by Seki who teach the application of either gold or platinum from the back of the substrate (layer 2; cf. column 3, lines 30-68 and column 4, line 1) to facilitate recombination of electrons and holes of this purpose in a vertical MOSFET. Although the device taught by Seki et al is not a trench type vertical MOSFET the same desirability of short turn-off time qualifies as a legitimate advantage and hence said purpose is valid for Applicants' invention as well, and hence motivation for combining the teaching by Seki with the teaching of the device of claim 4 exists. The standard gettering techniques as applied by Seki can be straightforwardly introduced in

the device as essentially taught by Mogi et al, Vinson and Darwish. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 4 at the time it was made so as to include the further limitation of claim 5.

4. ***Claim 9*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al, Vinson and Darwish as applied to claim 6 above, and further in view of Wolf et al (ISBN 0-9616721-6-1). As detailed above, claim 6 (on which claim 9 depends) is unpatentable over Mogi et al in view of Vinson and Darwish.

Neither Mogi et al nor Vinson nor Darwish necessarily teach the further limitation as defined by claim 9.

However, as explained in standard textbooks such as Wolf et al, the use of silicon oxynitride as semiconductor insulation layer has long been recognized to have the following advantages: the properties of silicon oxynitrides can be tailored, through the stoichiometric variables pertaining to the oxygen and nitrogen contents, to improve (a) thermal stability, (b) lower film stress, and (c) crack resistance.

All of the above three advantages have relevance for the gate insulating layer in the invention by Applicants. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 6 so as to include the further limitation as defined by claim 9.

5. ***Claim 25*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mogi et al (4,250,519), Vinson (4,116,720) and Darwish (6,569,738 B2) as applied to claim 1

above, and further in view of Baliga (ISBN: 0-89464-799-7) and van Loon et al (4,219,835). As detailed above, claim 1 (on which claim 25 depends) is unpatentable over Mogi et al in view of Vinson and Darwish, who do not necessarily teach the further limitation as defined by claim 25. However, it has long been known in the art to use source-body contact for the specific purpose to reduce second breakdown through a reduction in the voltage across the emitter-base junction of the parasitic bipolar transistor in MOSFET devices, as discussed in Baliga (page 318, second paragraph). Van Loon et al actually implement said source-body contact for the particular case of VMOSFET devices (cf. abstract, fourth sentence, column 2, lines 41-44 and column 3, lines 24-29).

Motivation to include the teaching by Baliga and van Loon et al in this regard into the invention as essentially taught by Mogi et al is the advantage to increase the breakdown voltage, which is commonly understood to be a generic advantage for all MOSFET devices. *Combination* of the aforementioned teachings with the aforementioned invention is straightforward through the implementation of a metal connection between source and body. *Success* in implementing said combination can therefore be reasonably expected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 31, 2003